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NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 03/09/2004

WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER

NHU, DAVID

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 03/09/2004

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/677,570

10/01/2003

Pete L. Pegler

LOVO-041.DIV

9290

TITLE OF INVENTION: METHOD FOR A JUNCTION FIELD EFFECT TRANSISTOR WITH REDUCED GATE CAPACITANCE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$0	\$1330	06/09/2004

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

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B. If the status is changed, pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above and notify the United States Patent and Trademark Office of the change in status, or

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B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.

☐ Applicant claims SMALL ENTITY status.
See 37 CFR 1.27.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

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Complete and send this form, together with applicable fee(s), to: **Mail**

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7590 03/09/2004

WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,570	10/01/2003	Pete L. Pegler	LOVO-041.DIV	9290

TITLE OF INVENTION: METHOD FOR A JUNCTION FIELD EFFECT TRANSISTOR WITH REDUCED GATE CAPACITANCE

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nonprovisional	NO	\$1330	\$0	\$1330	06/09/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
NHU, DAVID	2818	438-914000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1	_____
2	_____
3	_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

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Please check the appropriate assignee category or categories (will not be printed on the patent); ☐ individual ☐ corporation or other private group entity ☐ government

4a. The following fee(s) are enclosed:

- ☐ Issue Fee
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- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

- ☐ A check in the amount of the fee(s) is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

Director for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature)

(Date)

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This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Alexandria, Virginia 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Alexandria, Virginia 22313-1450.**

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10/677,570	10/01/2003	Pete L. Pegler	LOVO-041.DIV	9290
7590	03/09/2004		EXAMINER	
WAGNER, MURABITO & HAO LLP Third Floor Two North Market Street San Jose, CA 95113			NHU, DAVID	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 03/09/2004

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) system (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (703) 305-1383. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

Notice of Allowability	Application No.	Applicant(s)	
	10/677,570	PEGLER, PETE L.	
	Examiner	Art Unit	
	David Nhu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 10/01/03.
2. ☒ The allowed claim(s) is/are 17-36.
3. ☒ The drawings filed on 01 October 2003 are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 10/278,303.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|---|
| 1. <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 2. <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____ |
| 3. <input type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____ | 7. <input checked="" type="checkbox"/> Examiner's Amendment/Comment |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9. <input type="checkbox"/> Other _____ |



EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the change and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Abstract

Page 35, lines 8, 10, "comprising" should be -- including --

Specifications

Page 13, line 6, "n-channel JFET 200" should be -- n-channel JFET **300** -- See figure 3.

Drawings

Submit new figures 1-7.

REASONS FOR ALLOWANCE

2. Claims 17-36 are allowed.
3. The following is an examiner's statement of reasons for allowance: None of the references of record teaches or suggests as cited in claims 17, 22, 27, 32: forming an altered n-type epitaxial region below said plurality of well regions for extending depletion regions surrounding said plurality of p-type gate regions into said n-type epitaxial layer without compromising an active regions of said JFET (as cited in claim 1); forming an altered p-type epitaxial region below said plurality of well regions for extending depletion regions surrounding said plurality of n-type gate regions into said p-type epitaxial layer without compromising an active region of said JFET (as cited in claim 22); forming an altered epitaxial region below said p-type gate

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region for enlarging a depletion region surrounding said p-type gate region, wherein said altered epitaxial region comprises a lightly doped p- layer, wherein said lightly doped p- layer comprises a second dopant concentration less than that of said p-type gate region (as cited in claim 27); forming an altered epitaxial region below said n-type gate region for widening a enlarging region surrounding said n-type gate region, wherein said altered epitaxial region comprises a lightly doped n-layer, wherein said lightly doped n-layer comprises a second dopant concentration less than that of said n-type gate region (as cited claim 32).

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Pegler (6,696,706 B1): Structure and Method for a Junction Field Effect Transistor (JFET) with Reduced Gate Capacitance.

Yu (6,251,716): JFET Structure and Manufacture Method for Low on Resistance and Low Voltage Application.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Nhu , (571)272-1792. The examiner can normally be reached on Monday-Friday from 7:30 AM to 5:00 PM.

The examiner's supervisor, David Nelms can be reached on (571)272-1787.

Art Unit: 2818

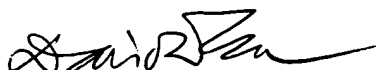
The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956

David Nhu



February 25, 2004



**DAVID NHU
PRIMARY EXAMINER**

STRUCTURE AND METHOD FOR A JUNCTION FIELD EFFECT TRANSISTOR
WITH REDUCED GATE CAPACITANCE

ABSTRACT OF THE INVENTION

5 An apparatus and method for a semiconductor device with
reduced gate capacitance. Specifically, an n-channel or
p-channel junction field effect transistor (JFET) is
described ^{including} ~~comprising~~ an appropriately doped substrate forming
a drain region, an epitaxial layer formed on top of the
10 substrate, a control structure ^{including} ~~comprising~~ a gate region
implanted into the epitaxial layer, a source region sharing a
p-n junction with the gate region, and an altered epitaxial
region. The altered epitaxial region is formed by implanting
either n⁻ or p⁻ dopants directly below the gate region of
15 either the n-channel or p-channel JFET for widening a
depletion region surrounding the gate region. The enlarged
depletion region reduces the gate capacitance of the JFET
between the gate and drain regions.

20

type gate region 210 maintains the same dimensions.
Correspondingly, the active region of the JFET device 200
remains unchanged.

5 Figure 3 is a cross section of a gate region 310 of an
n-channel JFET ~~200~~³⁰⁰ semiconductor structure with reduced
junction gate to drain capacitance, in accordance with one
embodiment of the present invention. The gate region 210 of
the n-channel JFET 200 can be repeated in a semiconductor
10 substrate to complete one or more n-channel JFET devices.

 The JFET 300 includes a heavily doped n^{++} substrate 320.
The n^{++} substrate 320 acts as the drain region for the JFET
300. Disposed on top of the n^{++} substrate 320 is an n-type
15 epitaxial layer 330. The dopant concentration of the n-type
epitaxial layer 330 is less than the n^{++} substrate 320. On
either side of a well region 350 are n^+ source regions 340
disposed on top of the n-type epitaxial layer 330. The
dopant concentration of the n^+ source regions is between that
20 of the n-type epitaxial layer 330 and the n^{++} substrate 320.

 The well region 350 is formed within the n-type
epitaxial layer 330 and provides access for the formation of
the p-type gate region 310. The p-type gate region 310 can
25 be formed through ion implantation, in one embodiment. In one
embodiment, the p-type gate region is formed by the masked
implantation of relatively heavy p^+ ions. Sidewall spacers,